Topography and Flatness Induced Overlay Distortion Correction using Resist Drop Pattern Compensation in Nanoimprint Lithography Systems

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Imprint lithography is a promising technology for replication of nano-scale features. For semiconductor device applications, Canon deposits a low viscosity resist on a field by field basis using jetting technology. A patterned mask is lowered into the resist fluid, which then quickly flows into the relief patterns in the mask by capillary action. Following this filling step, the resist is crosslinked under UV radiation, and then the mask is removed, leaving a patterned resist on the substrate.

Overlay budgets play a large role in defining production readiness. As an example, DRAM devices require overlay on the order of 20% of the half pitch. Canon uses a through the mask (TTM) alignment system to measure a Moiré image anywhere in the field. This system can also record alignment errors of all fields and all marks. The data collected by the TTM system correlates very closely with an Archer measurement tool. In addition, a High Order Distortion Correction (HODC) system, which applies a heat input on a field by field basis through the use of a DMD array has been combined with magnification actuators to correct high order distortion terms up to K30 (Figure 1).

There is an additional distortion term that must also be addressed for the case of nanoimprint lithography. NIL drop patterns are typically designed to minimize resist fill time and create a uniform residual layer beneath the resist pattern. For device wafers, however, it is important to recognize that there are both long wavelength flatness errors coming from the wafer chuck and existing pattern topography from previously patterned levels that cause out of plane errors. When the mask comes in contact with the resist on the wafer, these out of plane errors can then induce mask bending, resulting in an additional distortion term.

To minimize this distortion, a Drop Pattern Compensation (DPC) Model has been implemented to minimize the added distortion terms. In this paper we describe the origins of the out of plane errors, and describe the model used to correct these errors along with some examples. Finally, results are presented for a device like wafer in which the overlay errors within a field are reduced from 5.4nm to 3.4nm, 3 sigma (Figure 2).

As time permits, an overview on the status of NIL for the manufacturing of advanced semiconductor devices will also be presented and will include topics such as throughput and defectivity. Finally, a roadmap for manufacturing, based on device type, will be discussed.

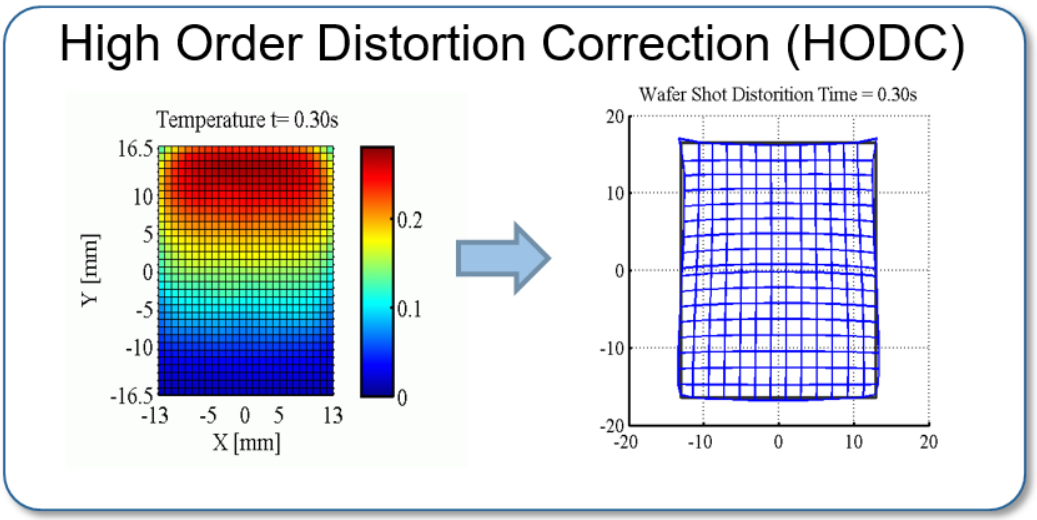

Figure 1. High Order Distortion Correction: Heat input is applied on a field by field basis through the use of DMD array.

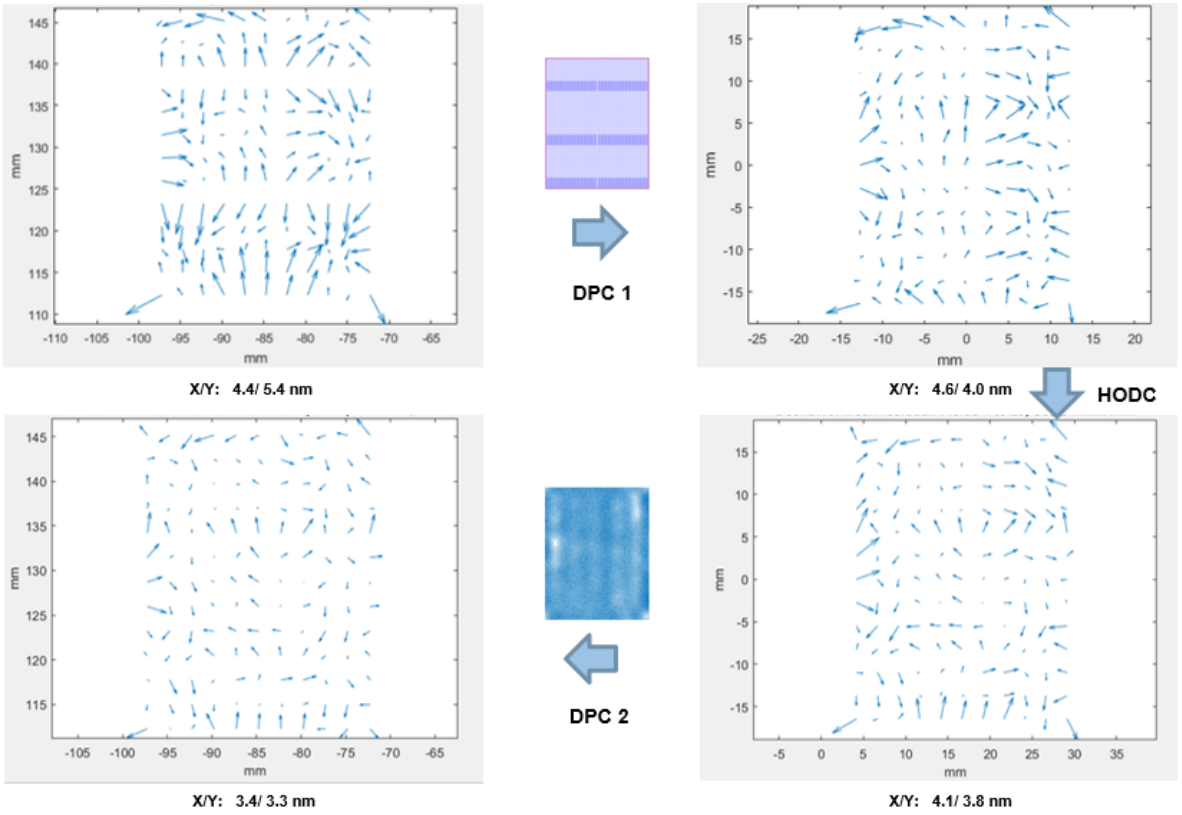

Figure 2. Demonstrates how DPC improves OL distortion for a device-like wafer. In this example, mix and match overlay (MMO) was originally 5.4nm. When a first DPC model is used, overlay reduces the error down to 4.6nm. After applying HODC, the error was further reduced to 4.1nm. A final DPC process achieves 3.4nm MMO.