

Manufacturing assessment of sub 100 nm features in Si/SiO₂ substrates based on EVG nanoimprint solution for 8 inch substrates

Hubert Teyssède¹, Florian Delachat¹, Manuela Stirner², Jonas Khan², Alain Campo¹, Fabrice Koueméni Tchouake¹, Peter Ledel², Mustapha Chouiki²

¹CEA-LETI, Minatec Campus, 17 rue des martyrs Grenoble, 38054 Cedex 9, France

²EV Group E.Thallner GmbH, DI Erich Thallner Str. 1, 4782 St. Florian am Inn, Austria

E-mail of corresponding author: hubert.teyssedre@cea.fr

NanoImprint techniques stick out from other more conventional lithography processes (photolithography, electronic lithography, EUV lithography) by virtue of the fundamental mechanisms that create the structures. With conventional approaches the structures are created through a chemical contrast, whereas a topographic one is formed in the case of NanoImprint thanks to the flow of the resist through the stamp's cavities.

In twenty years, consequent technical developments have been achieved to make the technology more mature [1,2]. Among a plenty of technology alternatives, the UV-based imprint, using transparent stamp, became the standard technology. Two well established options are now available on the market: the full wafer imprint [3] (the size of the stamp correspond to the size of the wafer to be printed) and the step and flash imprint [4] where a small stamp (i.e. die size) is stepped across the wafer to be processed.

If the step and flash technology has demonstrated its capabilities to address the semiconductor markets with high-requirement levels for alignment capability and defectivity density, the full wafer option seems to be the reference for the emerging and growing markets like LED and Photonics based devices having lower defectivity level requirements. To fulfill the market needs, some items of the supply chain such as the imprint materials, the imprint equipment and the compatibility of the NIL process with an integration process flow need to be qualified in a manufacturing like environment.

In this paper we evaluate a lithography and etch step of Si/SiO₂ 8 inch substrates based on the EVG SmartNIL tool and EVG NIL materials solution. The evaluation is performed on a set of contact arrays, with the layout presented in figure 1, with variable diameters (from 100 to 50 nm) and variable densities (from 1:3 to 1:15) and line and space arrays with a density of 1:4 and variable spaces widths (from 100 to 50 nm) for 25 wafers imprinted in a single run. The process uses the EVG AS2 soft stamp material and the EVG UVA series imprint material, both being processed at room temperature and cured with 365 nm UV LED lamp. Based on CDSEM characterizations, automated dark field inspections and SEM cross-sections, we demonstrate that this process, qualified in 2017 [5] for features bigger than 500 nm period and shallow aspect ratio, can now be used to replicate sub 100 nm features with high fidelity, as presented in figure 2. Furthermore, we discuss the process window of the process and its compatibility with high volume manufacturing for photonic applications and we point out the specific developments made around the nanoimprint such as priming, etching and stripping of the substrates and the perspectives for 3D patterning.

References:

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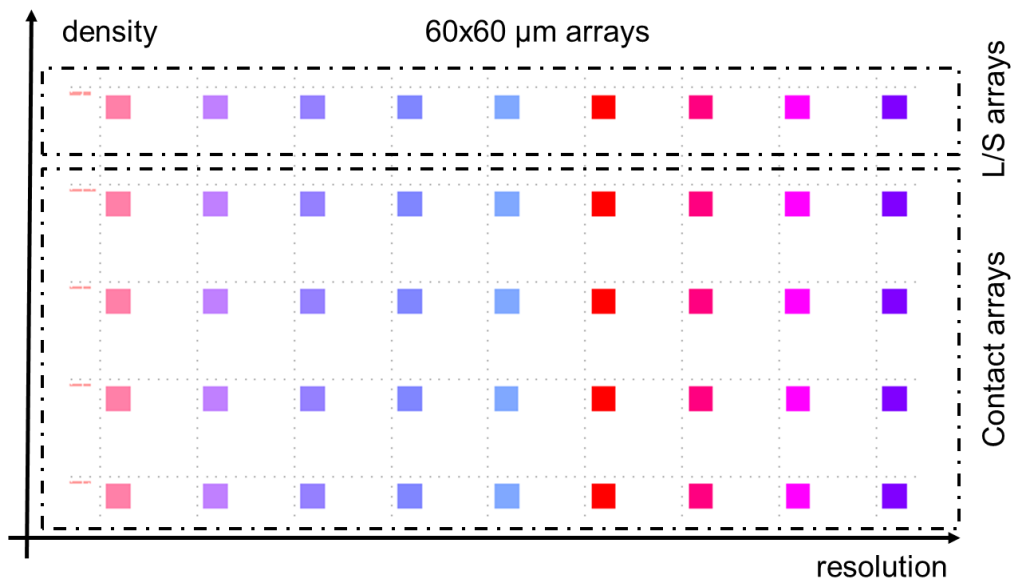


Figure 1. Master layout used for NIL technology assessment. The layout is composed of 60x60 μm arrays for single designs (line and space or contact holes). The densities from one array to the other varie between 1:3 to 1:15 and the critical dimensions between 100 and 50 nm. This layout is repeated on a full 8 inch master with a depth of 125 nm.

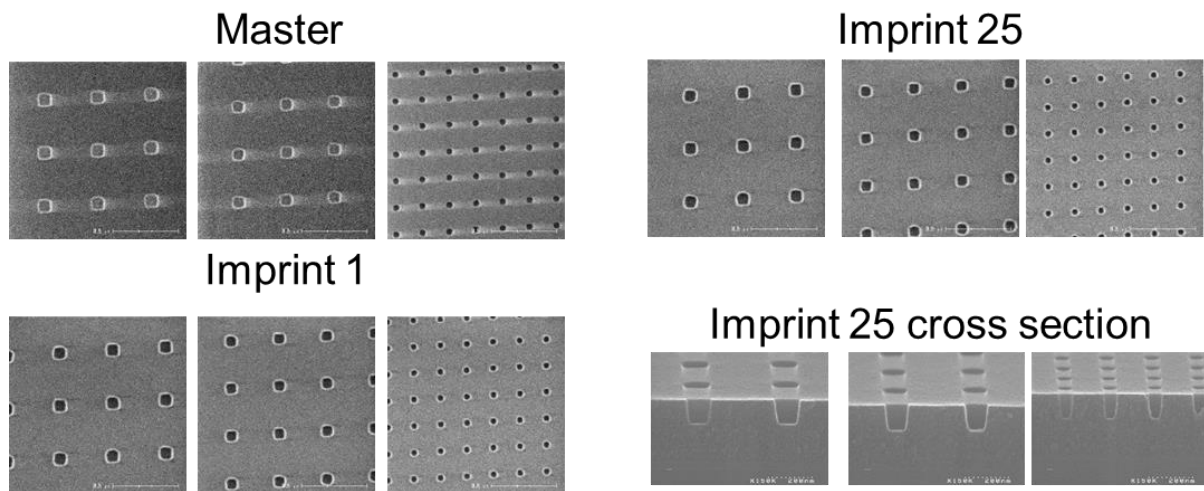


Figure 2. CDSEM to view and cross sections of 1:3 contacts array for 100, 90 and 50 nm designs from master, imprint 1 and imprint 25.